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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	PROD. REL PER E.O. 00009	9-5-78	JLR
H	REVISED PER E.O. 00144	12-20-79	JLR

REF. ONLY

2. ALL CAPACITORS ARE IN MICRO-FARADS.  
1. ALL RESISTORS ARE 1/4W, 5%.
- NOTES: UNLESS OTHERWISE SPECIFIED.

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES		± ± ±	
APPROVALS	DATE				
DRAWN JRT	10-13-77				
CHECKER	10-13-77				
SCALE		SIZE		DRAWING NO.	
		B		10015003	
DO NOT SCALE DRAWING				SHEET 1 OF 15	

ACT

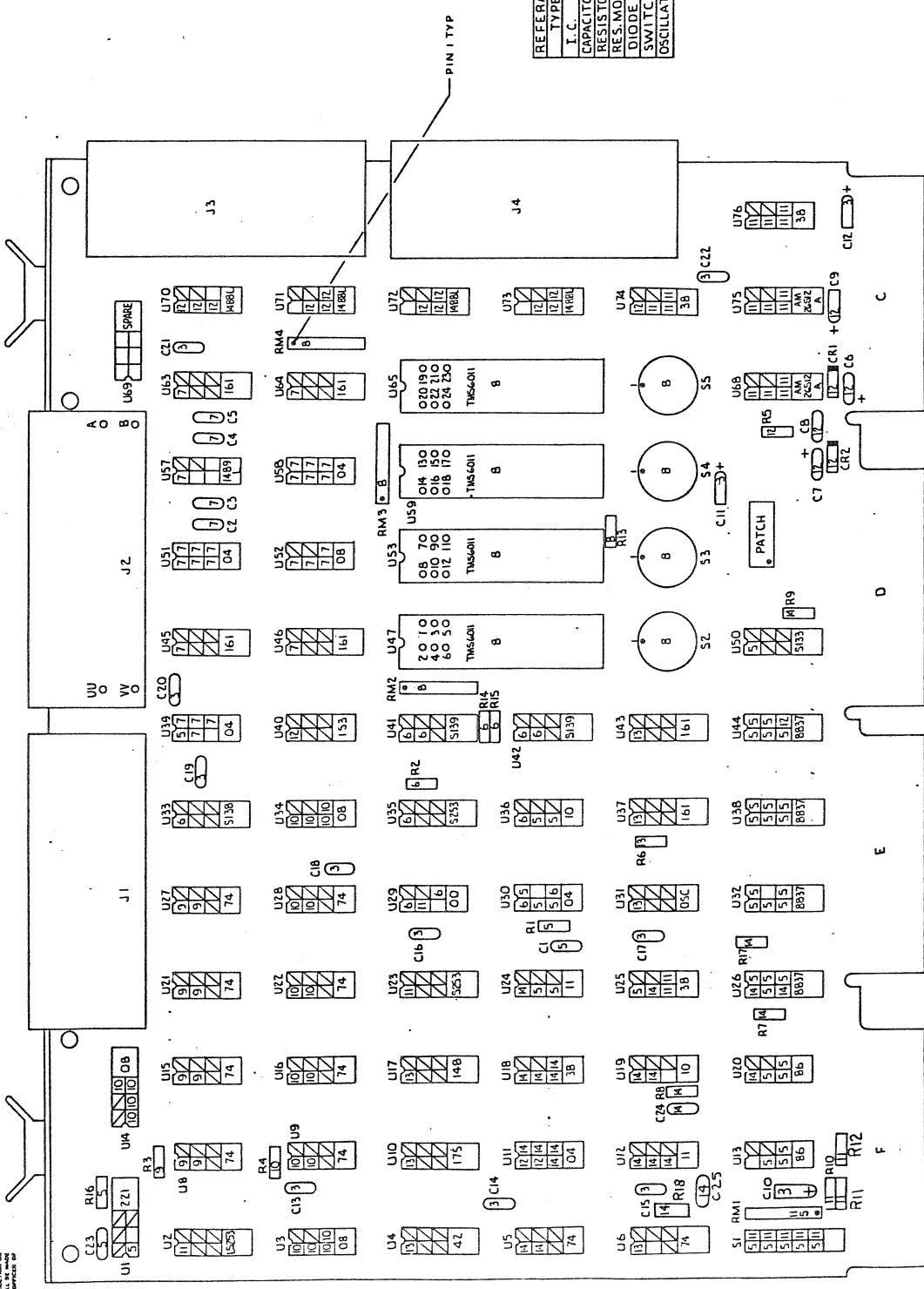
ABLE COMPUTER TECHNOLOGY

SCHEMATIC

QUADRASYNC / B

REV	DESCRIPTION	DATE	APPROVED
1	SEE SHT. 1		

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REFERENCE DESIGNATION CHART		
TYPE	LAST USED	NOT USED
I.C.	U 76	
CAPACITOR	C 25	
RESISTOR	R 18	
RES. MOD.	RM 4	
DIODE	CR 2	
SWITCH	SS	
OSCILLATOR	U 51	

PROJECT NAME		ART Computer Technology	
PROJECT NUMBER		SCHEMATIC - QUADRA SYNC / B	
DATE	10/11/77	SCALE	D 10015003
DRAWN BY		DO NOT SCALE DRAWING	

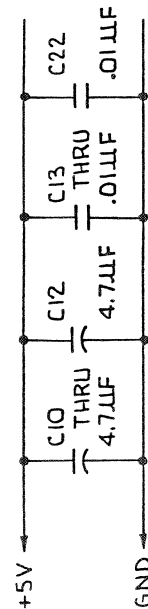
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SHT	2	F	I	SHT
	+5V	A		
	GND	B		
		C	BUS-SSYN-L	5
		D	BUS-88SY-L	14
		E		
		F		
		H		
		J		
		K		
		L		
		M	BUS-INTR-L	14
		N		
		P		
		R		
		S		
14	BUS-SACK-L	T		
		U		
		V		

SHT	2	E	I	SHT
	+5V	A		
		B		
5	GND	C	A12-L	5
5	A15-L	D	A17-L	5
5	A16-L	E	BUS-MSYN-L	5
5	C1-L	F	A02-L	5
5	A00-L	H	A01-L	5
5		J		
5	A13-L	K	A14-L	5
		L	A11-L	5
		M		
5	A08-L	N		
5	A07-L	P	A10-L	5
		R	A09-L	5
		S		
		T		
5	A04-L	U	A06-L	5
5	A03-L	V	A05-L	5

SHT	2	D	I	SHT
	+5V	A		
		B		
	GND	C		
15	BR7-L	D		
15	BR6-L	E		
15	BR5-L	F		
15	BR4-L	H		
		J		
15	BG7-IN	K		
15	BG7-OUT	L	BUS-INIT-L	12
15	BG6-IN	M		
15	BG6-OUT	N		
15	BG5-IN	P		
15	BG5-OUT	R		
15	BG4-IN	S		
15	BG4-OUT	T		
		U		
		V		

SHT	2	C	I	SHT
	+5V	A		
12	-15VDC	B		
	GND	C		
		D		
		E		
		F		
		H		
		J		
		K		
11	D08-L	L		
11	D07-L	M		
11	D04-L	N		
11	D05-L	P		
11	D01-L	R		
11	D00-L	S		
11	D03-L	T		
11	D02-L	U	+V	
11	D06-L	V		12



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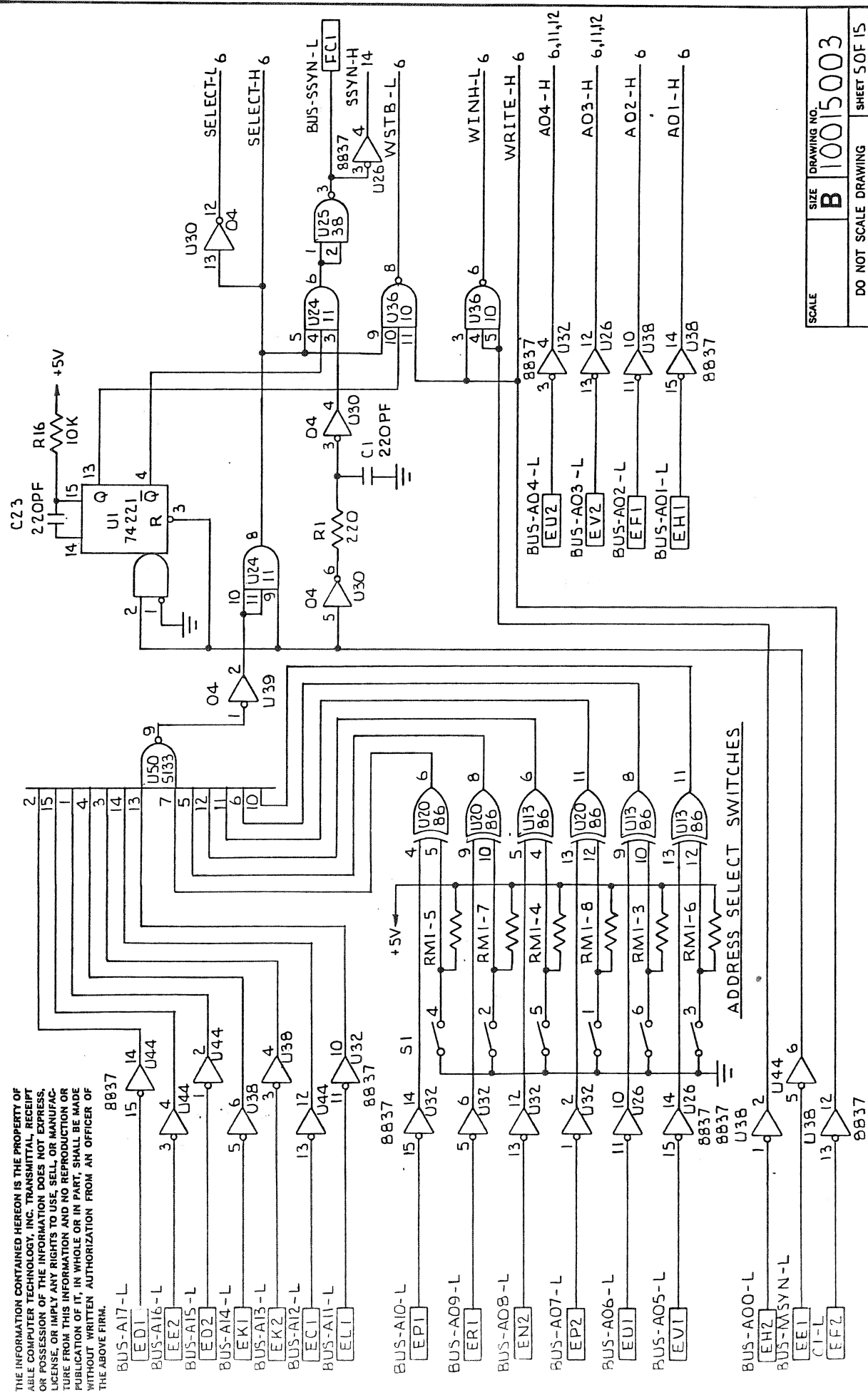
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	GND	1 UU	VV 2	GND	
		3 SS	TT 4	+5V	
		5 PP	RR 6		
		7 MM	NN 8		
		9 KK	LL 10		
		11 HH	JJ 12		
		13 EE	FF 14		
		15 CC	DD 16	RDY-1	12
		17 AA	BB 18		
		19 Y	Z 20		
		21 W	X 22		
		23 U	V 24	SEND-1	12
		25 S	T 26		
		27 P	R 28		
		29 M	N 30		
		31 K	L 32		
		33 H	J 34	REC DATA-1	7
		35 E	F 36	DATA-1	12
		37 C	D 38		
	GND	39 A	B 40	GND	

SHT	J 3				SHT
	GND	1 UU	VV 2	GND	
		3 SS	TT 4	+5V	
		5 PP	RR 6		
		7 MM	NN 8		
		9 KK	LL 10		
		11 HH	JJ 12		
		13 EE	FF 14		
		15 CC	DD 16	RDY-3	12
		17 AA	BB 18		
		19 Y	Z 20		
		21 W	X 22		
		23 U	V 24	SEND-3	12
		25 S	T 26		
		27 P	R 28		
		29 M	N 30		
		31 K	L 32		
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		35 E	F 36	DATA-3	
		37 C	D 38		
	GND	39 A	B 40	GND	

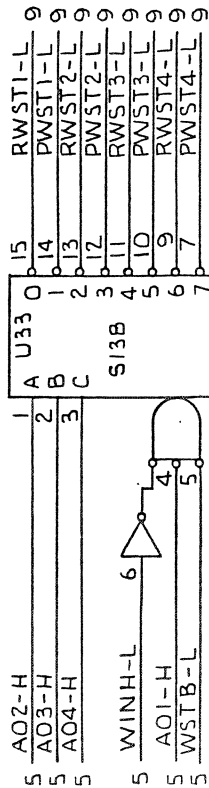
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	GND	1 UU	VV 2	GND	
		3 SS	TT 4	+5V	
		5 PP	RR 6		
		7 MM	NN 8		
		9 KK	LL 10		
		11 HH	JJ 12		
		13 EE	FF 14		
		15 CC	DD 16	RDY-2	12
		17 AA	BB 18		
		19 Y	Z 20		
		21 W	X 22		
		23 U	V 24	SEND-2	12
		25 S	T 26		
		27 P	R 28		
		29 M	N 30		
		31 K	L 32		
		33 H	J 34	REC-DATA-2	7
		35 E	F 36	DATA-2	12
		37 C	D 38		
	GND	39 A	B 40	GND	

SHT	J 4				SHT
	GND	1 UU	VV 2	GND	
		3 SS	TT 4	+5V	
		5 PP	RR 6		
		7 MM	NN 8		
		9 KK	LL 10		
		11 HH	JJ 12		
		13 EE	FF 14		
		15 CC	DD 16	RDY-4	12
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		19 Y	Z 20		
		21 W	X 22		
		23 U	V 24	SEND-4	12
		25 S	T 26		
		27 P	R 28		
		29 M	N 30		
		31 K	L 32		
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	GND	39 A	B 40	GND	

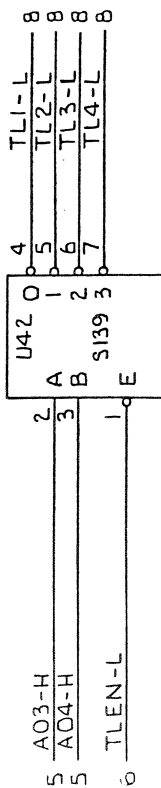
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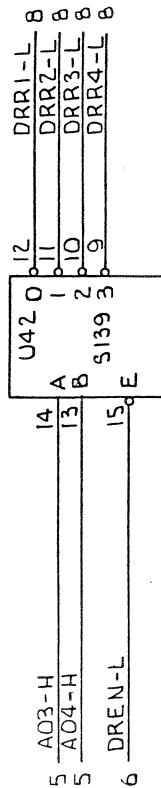
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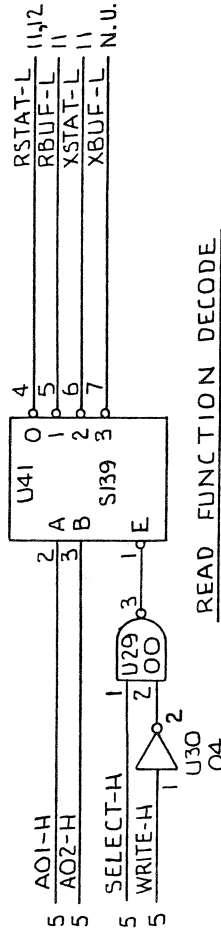
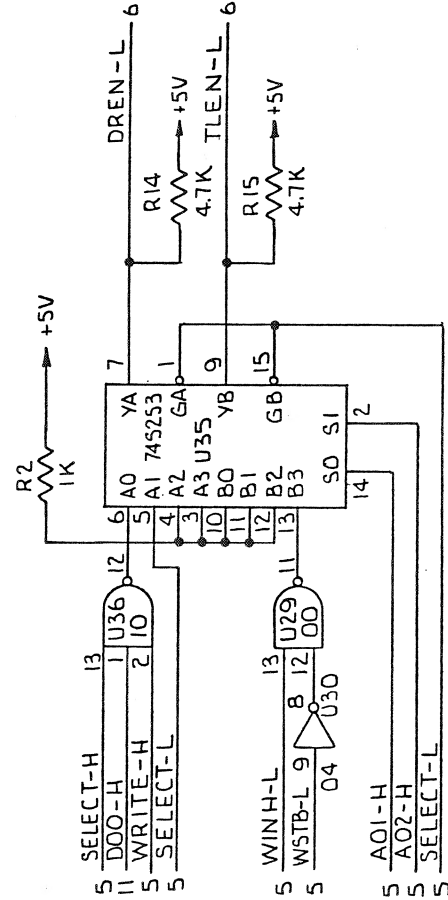
#### READ/XMITTER STATUS CLOCKS



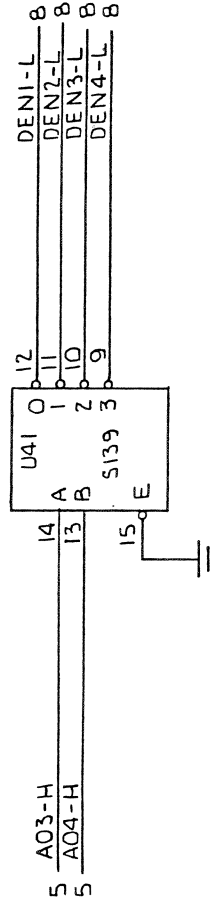
#### XMITTER LOAD CLOCKS



#### DATA READY RESET

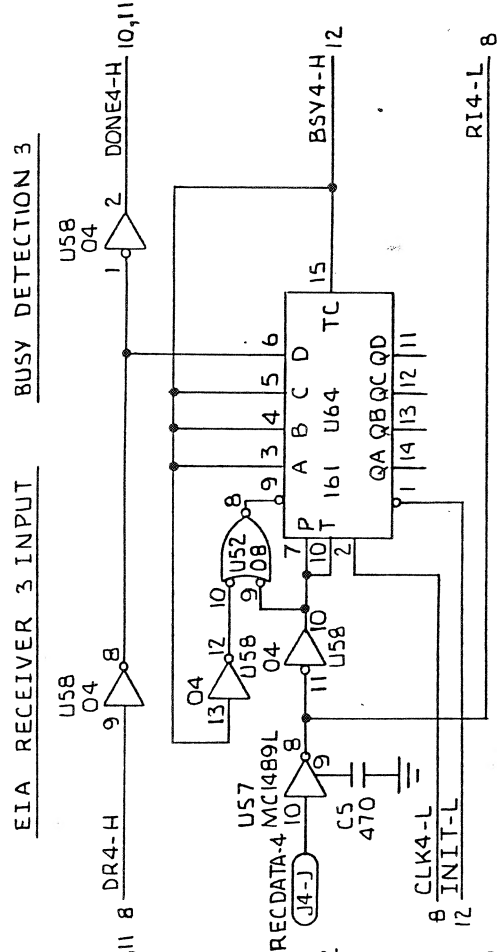
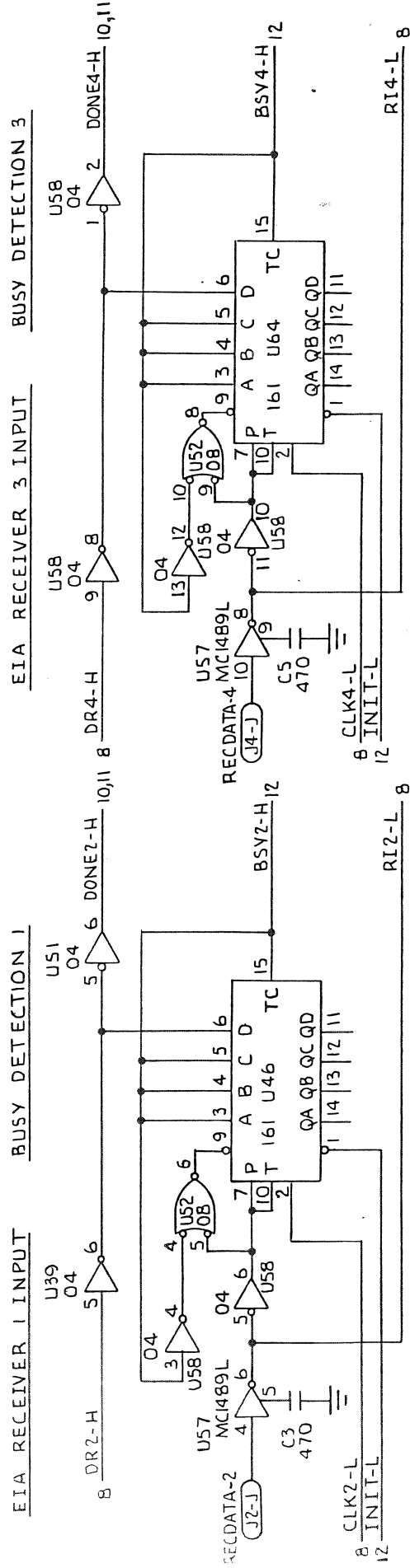
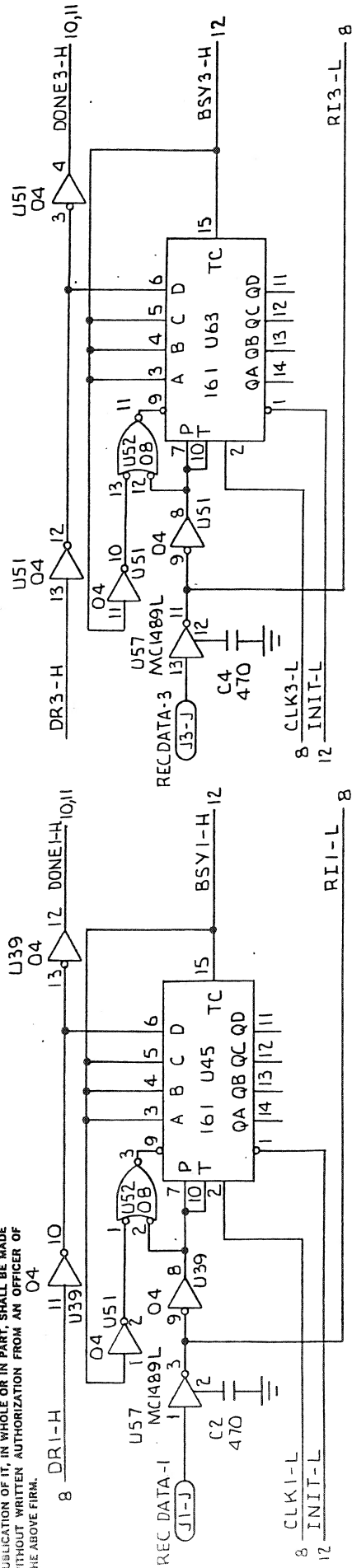


#### READ FUNCTION DECODE



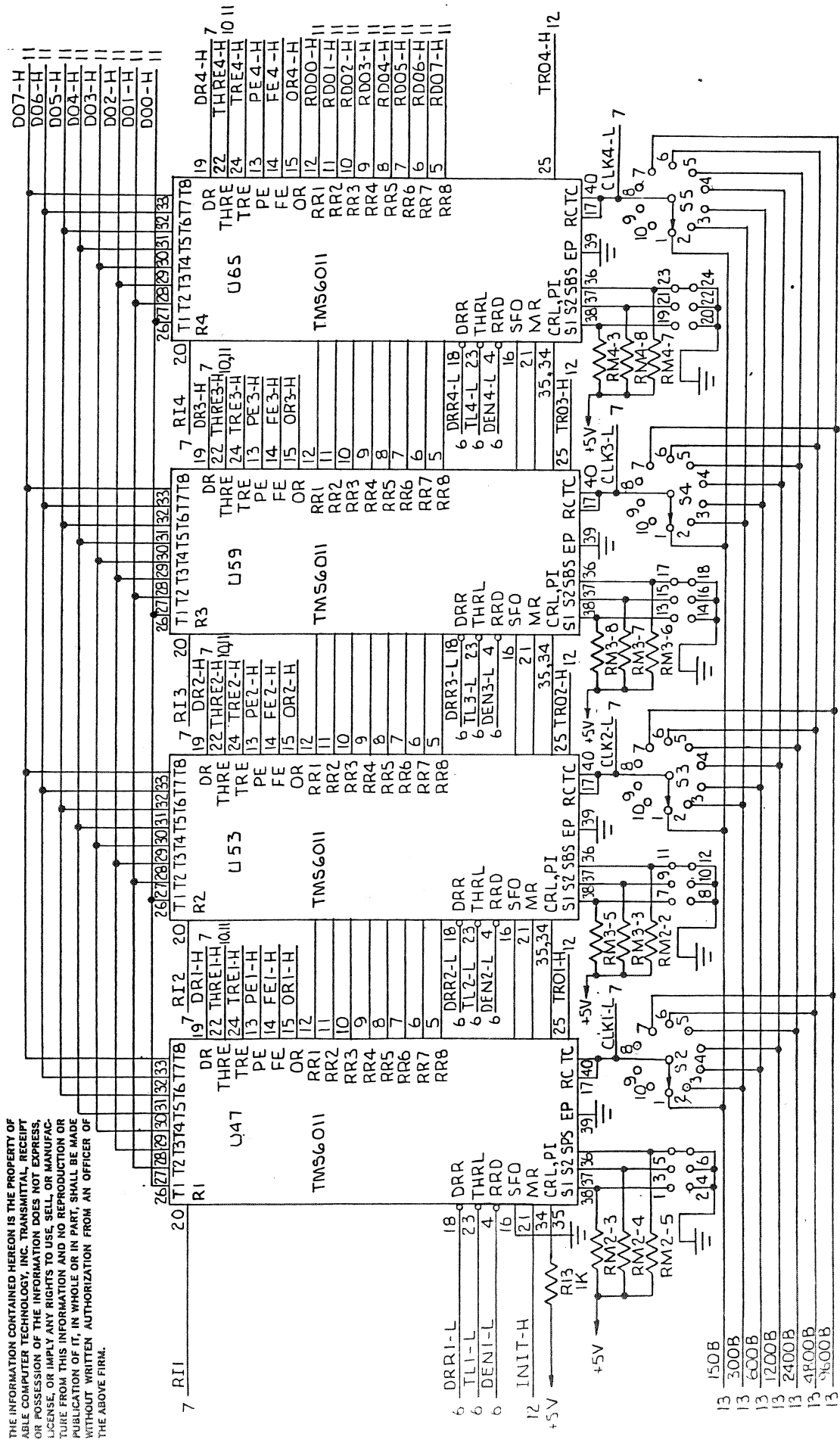
#### DATA ENABLE STROBES

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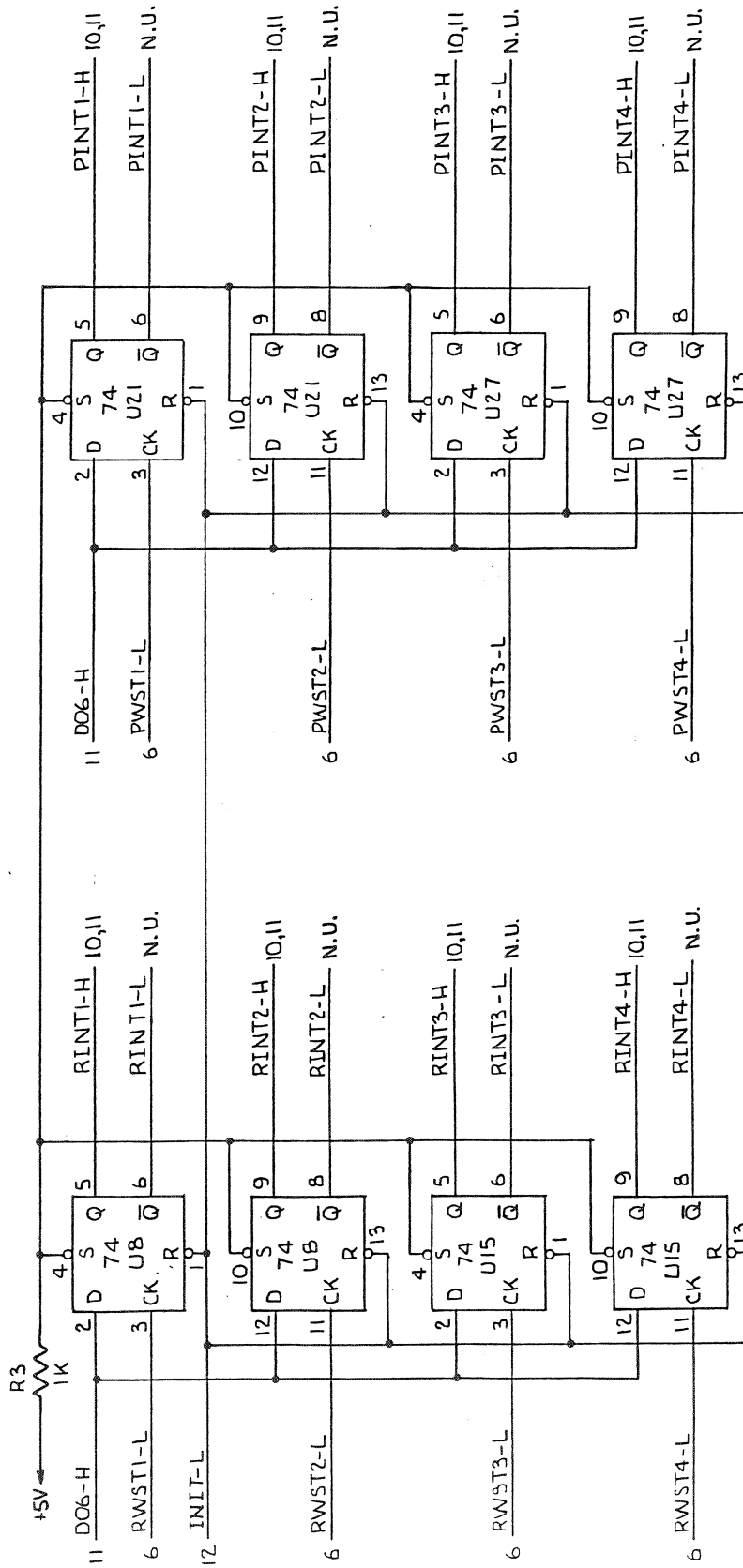
EIA RECEIVER 4 INPUT      BUSY DETECTION 4

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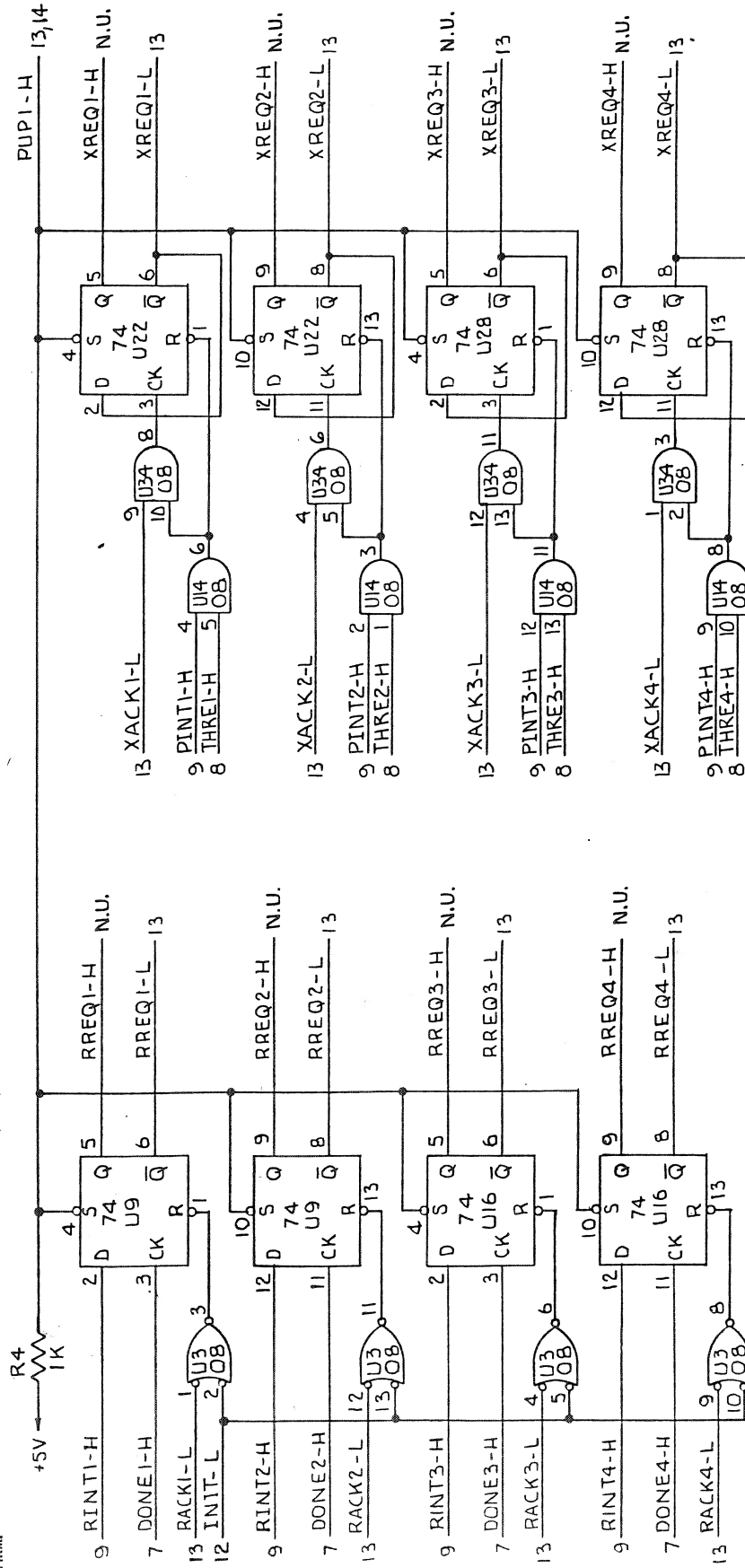
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RECEIVER INTERRUPT ENABLE

XMITTER INTERRUPT ENABLE

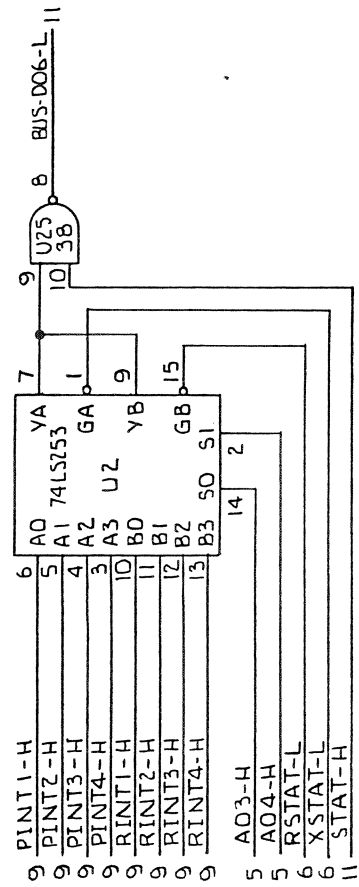
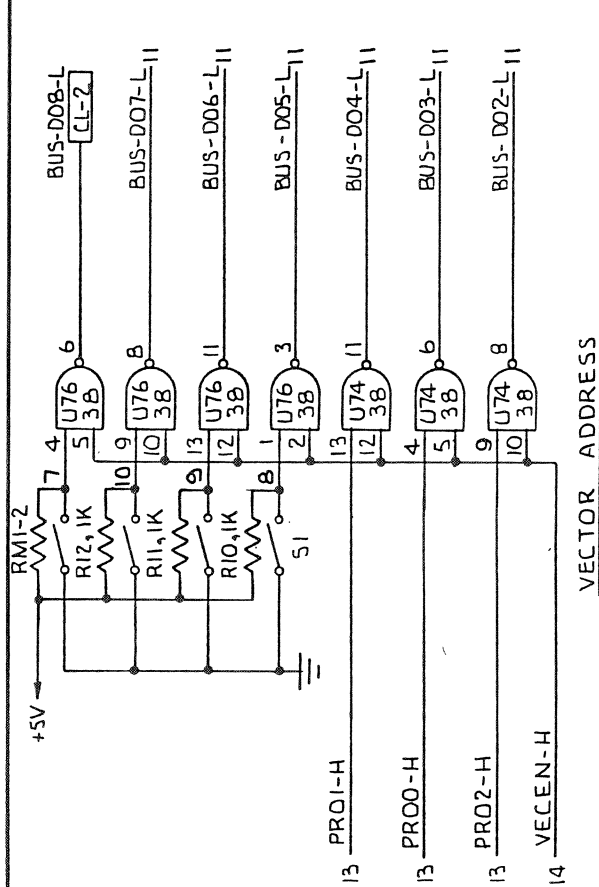
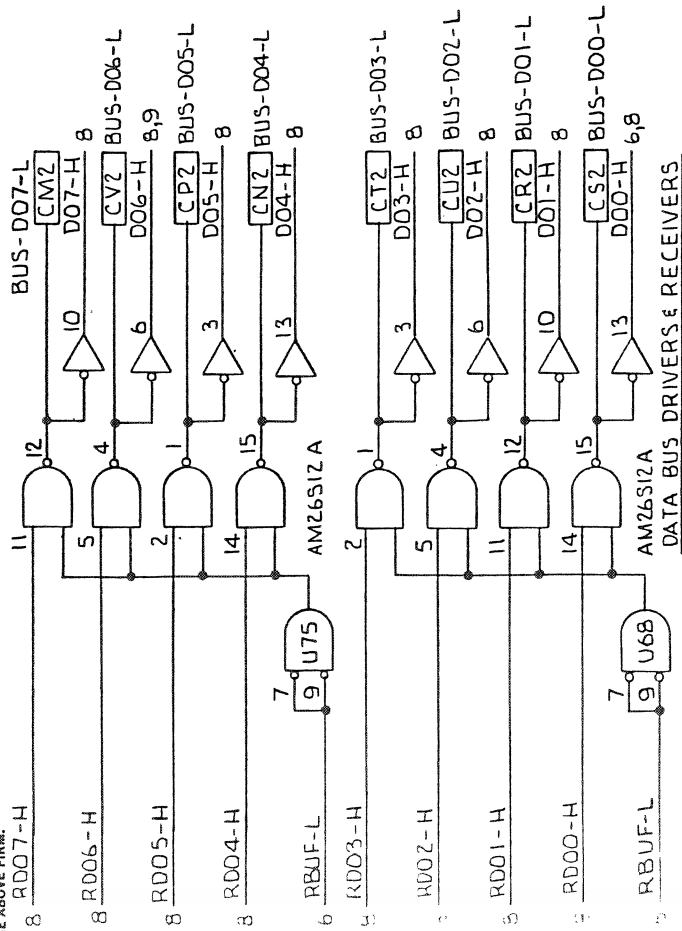
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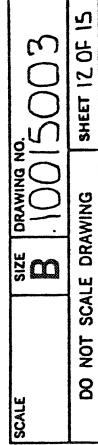


RECEIVER INTERRUPT REQUEST

TRANSMITTER INTERRUPT REQUEST

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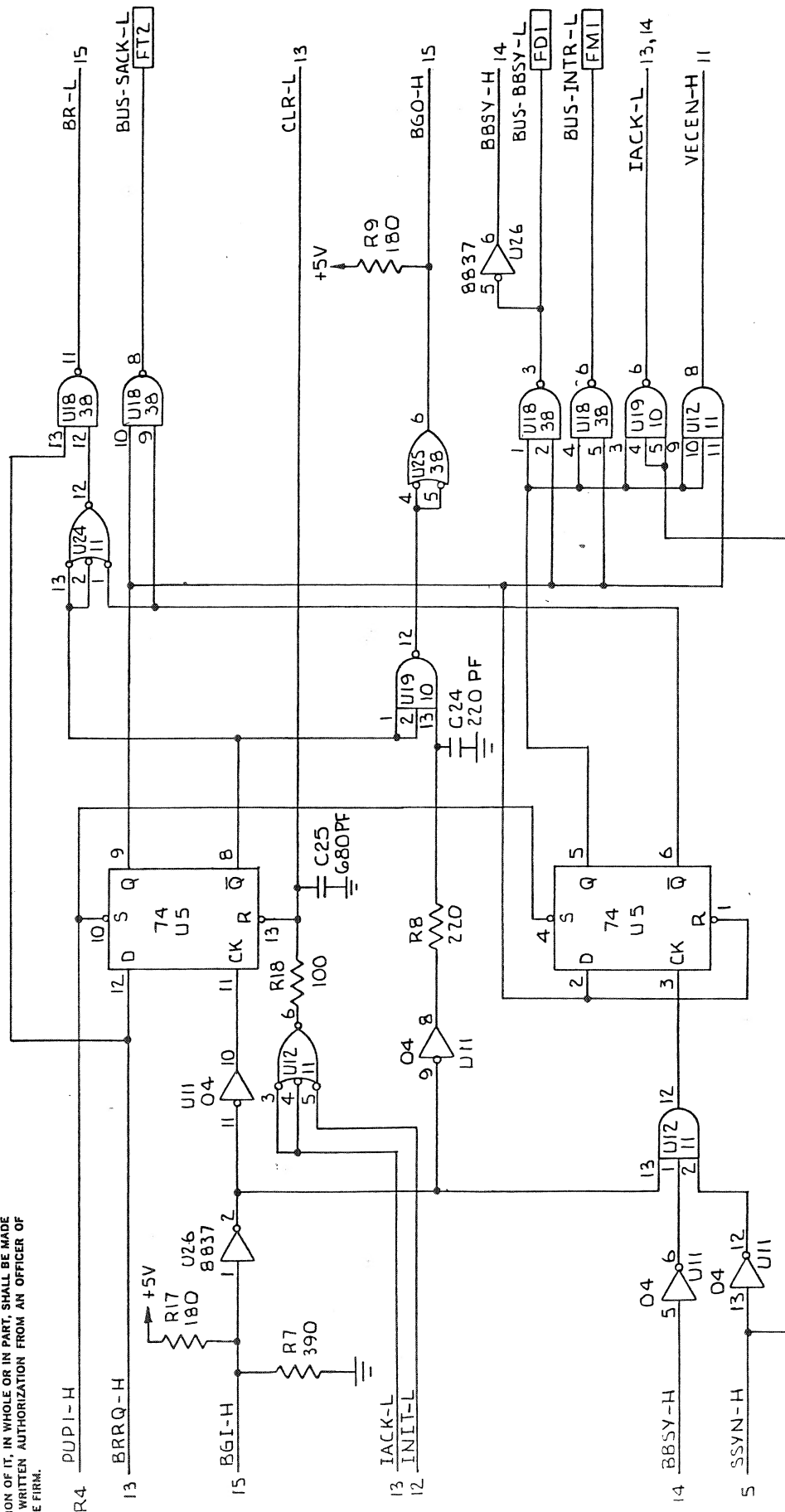


[illegible]

[illegible]

SCALE	SIZE	DRAWING NO.
	B	10015003

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# INTERRUPT CONTROL

SCALE	SIZE	DRAWING NO.
	B	10015003
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BR / BG LEVEL SELECT

PATCH